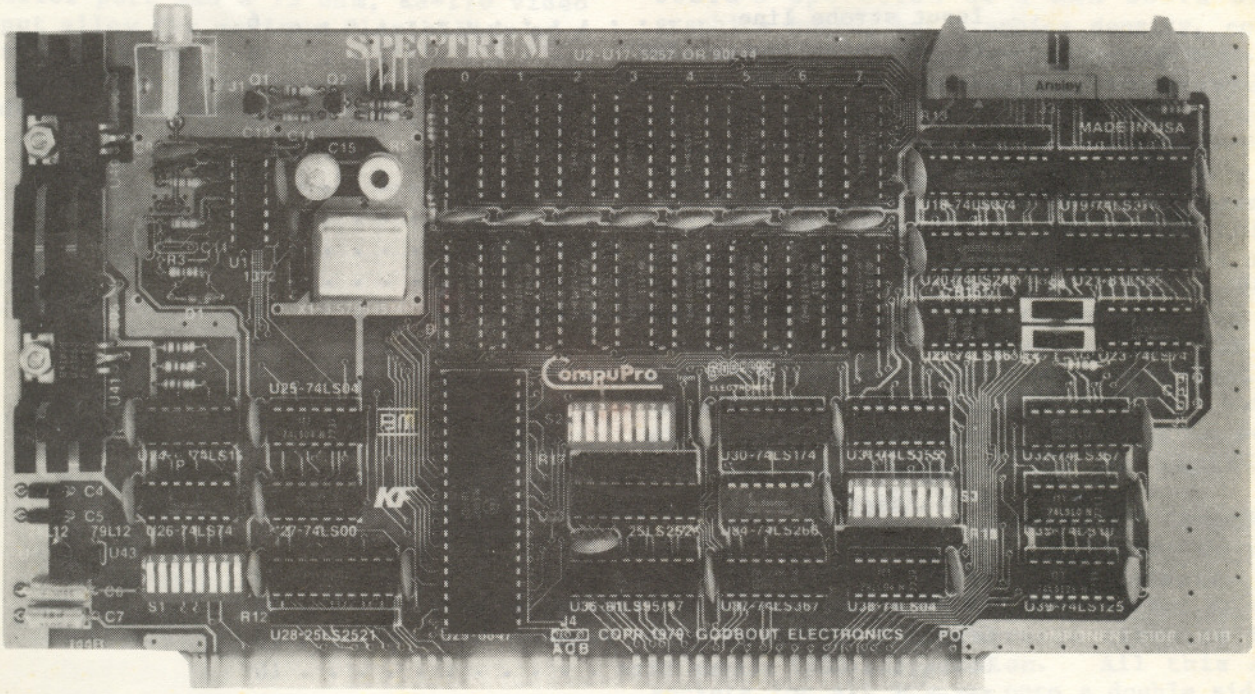
SPECTRUM™

USER MANUAL



IEEE 696 / S-100

FULL FUNCTION GRAPHICS BOARD

With 8K RAM & Parallel I/O

Using 6847

144E

mac

CompuPro™ division GODBOUT ELECTRONICS

5/81

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ABOUT SPECTRUM

Congratulations on your purchase of SPECTRUM - a color graphics board designed specifically for full electrical and mechanical compatibility with the IEEE S-100 bus standard. The S-100 bus is the professional level choice for commercial, industrial and scientific applications. This bus provides for ready expansion and modification as the state of the computing art improves. We believe that this board with the rest of the S-100 portion of the CompuPro family is one of the best boards available for that bus.

Features, such as 8K of fast, low power static RAM, 24 bit addressing, a full duplex parallel port and a 75 ohm, RS-170 video output allow for maximum flexibility at a reasonable price.

Thank you for choosing a CompuPro Product.... welcome to the club.

TECHNICAL OVERVIEW

This board incorporates proven static memory technology for the 8K x 8 screen memory of the 6847 color graphics generator. With the 6847, the user can select 10 different color modes of operation - from full alphanumerics with semigraphics to high density graphics.

Upon power-up, the SPECTRUM board behaves as a standard high speed 8K static RAM board - capable of running at 6MHz with a Z-80 and 8MHz with an 8085 or 8088. When graphics are required, the user alters the board programming through the Graphics Control Port. This port not only controls the board's operation as a RAM board or a graphics board, but graphics density, color set and alphanumerics/semi-graphics mode.

A 75 ohm video output is provided through an RCA type jack for direct connection to a color monitor, or through a four pin connector that can directly mate to any F.C.C. approved modulator. A programmable wait state is provided in color graphics mode to compensate for the restricted timing requirements when the 6847 is in operation. 24 bit addressing is provided so that the graphics RAM can be removed from base page memory, and finally, a full duplex parallel port with full handshaking is provided for interfacing to keyboards, joysticks, LED's or anything requiring parallel data.

Other features standard to all CompuPro boards include thorough bypassing of all supply lines to suppress transients, on board regulators, and low power Schottky and MOS technology integrated circuits for reliably cool operation. All this and sockets for all IC's go onto a double sided, solder masked printed circuit board with a complete component layout legend.

MEMORY ADDRESS ASSIGNMENT

This board is addressable as one single 8K block, positionable on any 8K boundary as shown below.

The RAM on this board can be disabled and electrically removed from memory space by placing switch S3-4 in the ON position. For normal operation, switch S3-4 should remain OFF.

SWITCH POSITION	FUNCTION
S3-1	ADDRESS A15
S3-2	ADDRESS A14
S3-3	ADDRESS A13
S3-4	MEMORY DISABLE
S3-5	WRITE ENABLE
S3-6	PHANTOM ENABLE
S3-7	PHASE 2 CLOCK SELECT
S3-8	WAIT STATE DISABLE

STARTING ADDRESS	SWITCH POSITION S3-1	S3-2	S3-3
0000H	ON	ON	ON
2000H	ON	ON	OFF
4000H	ON	OFF	ON
6000H	ON	OFF	OFF
8000H	OFF	ON	ON
A000H	OFF	ON	OFF
C000H	OFF	OFF	ON
E000H	OFF	OFF	OFF

EXAMPLE: To address the **SPECTRUM** board at C000H for use with the Universal Graphics Interpreter, you would place S3-1, and S3-2 in the "OFF" position, and S3-3 in the "ON" position. Position S3-4 should be "OFF".

WRITE ENABLE SWITCH

Switch position S3-5 can be used to write protect the 8K block of memory. With S3-5 in the "OFF" position, the contents of the memory can be read, but cannot be written into. For normal operation, this switch should remain "ON".

PHANTOM SWITCH

Switch position S3-6 can be used to PHANTOM the memory on this board out of memory space. With S3-6 in the "ON" position, a low level on the PHANTOM* line (pin 67) will disable the 8K block. For operation of this board in a mode where PHANTOM* has no effect, S3-6 should be kept "OFF".

WAIT STATE SWITCH

Switch position S3-8 is used to disable the wait state circuit when running in graphics mode. In 2MHz systems, this board is fast enough to run with no wait states - even in graphics mode. However, in systems running at greater than 4 or 5MHz, a wait state is required in graphics mode to insure reliable data transfer. Therefore, 2MHz systems should run with S3-8 in the "ON" position (wait state disabled), and 4MHz and up systems should have S3-8 turned "OFF" and the proper clock phase selected with S3-7. This board should run with zero wait states in RAM mode in any high speed system.

With the wait state enabled, S3-7 should be set to provide the proper clock phase to the wait state generator. Typically, S3-7 should be in the "OFF" position when used with most S-100 standard CPU boards. However, some of the older processors might require it in the "ON" position. If you are getting reliable data transfers at greater than 3 MHz, S3-7 is probably in the right position.

S3-7	CLOCK PHASE
ON	NORMAL PHASE 2 CLOCK
OFF	INVERTED PHASE 2 CLOCK

EXTENDED 24 BIT ADDRESSING

This board implements the proposed IEEE S-100 extended address lines A16 thru A23. With this feature, the user can place the RAM on this board in a location other than base page. As shipped, this board is set to use the extended address lines when decoding the board's location in the memory map. To disable this feature, a jumper must be installed at location J2 (in between U26 and U27 in the lower left corner of the board. When disabled, we suggest that you remove U28 (25LS2521) and place all 8 switches of S1 in the "OFF" position. Addressing is as shown below.

SWITCH POSITION	FUNCTION	
S1-1	ADDRESS A23	
S1-2	ADDRESS A22	
S1-3	ADDRESS A21	"ON" = "0"
S1-4	ADDRESS A20	
S1-5	ADDRESS A19	"OFF" = "1"
S1-6	ADDRESS A18	
S1-7	ADDRESS A17	
S1-8	ADDRESS A16	

EXAMPLE: To address this board in extended page "0" (base page), all eight positions of S-1 should be "ON".

EXAMPLE: To address this board in extended page "0F" (high memory for an 8088), positions 1 through 4 of S1 should be "ON", and positions 5 through 8 should be "OFF".

NOTE: It is not necessary to install jumper J2 in a system that does not generate extended addresses. The user may instead simply set switch S1 to match the state of the dormant extended address lines (usually all "OFF").

PORT ADDRESS SELECTION

The SPECTRUM board contains two I/O ports to increase its flexibility. A full duplex parallel port (8 lines "IN" and 8 lines "OUT") is provided to interface to any type of parallel device. In addition, a Status/ Control port is provided to observe the status of the parallel port and the graphics chip, and control the modes of the graphics display.

Switch S2 is used to select the address of the two ports, with the pair addressable at any location in the I/O map on any two port boundary. The Status/ Control port resides at the selected address on S2, and the Data port resides at the selected address + 1.

SWITCH POSITION	FUNCTION	
S2-1	ADDRESS A7	
S2-2	ADDRESS A6	
S2-3	ADDRESS A5	"ON" = "0"
S2-4	ADDRESS A4	
S2-5	ADDRESS A3	"OFF" = "1"
S2-6	ADDRESS A2	
S2-7	ADDRESS A1	
S2-8	PORT DISABLE	"ON" = DISABLED

EXAMPLE: If the ports are set for F0H (1-4 and 8 "OFF", 5-7 "ON"), then the Status/ Control port will be at port F0H, and the Data port will be at port F1H.

EXAMPLE: If the ports are set for 80H (1 and 8 "OFF", 2-7 "ON") for use with the subLOGIC Universal Graphics Interpreter, then the Status/Control port will be at port 80H, and the Data port will be at port 81H.

STATUS/CONTROL PORT BIT ASSIGNMENT

The bit assignment for the STATUS and CONTROL ports are as shown below. In depth descriptions of these bits will be covered in further sections. The STATUS word is read from the SPECTRUM board, and the CONTROL word is written to the SPECTRUM board.

DATA BIT	STATUS WORD (when read)	CONTROL WORD (when written)
D0	DAV	GM0
D1	DNT	GM1
D2	UNDEF.	GM2
D3	UNDEF.	A*/G
D4	UNDEF.	CSS
D5	UNDEF.	R*/G
D6	HS*	UNDEF.
D7	FS*	UNDEF.

DATA LINES

The parallel channel on this board provides 8 input lines and 8 output lines for the user.

The 8 input lines (DI0-DI7) allow a full byte of TTL level data to be sampled by the processor through the INPUT DATA register. All 8 data lines as well as the STROBE line are pulled to 5 volts through the pull-up resistors in SIP R13, and are therefore considered as a logic "1" if left disconnected.

The 8 output lines (DO0-DO7) are not only capable of sinking 24 Ma., but can be tri-stated through the use of the OUTPUT ENABLE LINE as described below. When new data is strobed into the output register by the processor, it is reflected on the ATTENTION LINE also described below.

INPUT STROBE LINES

The STROBE line on the input Channel is used to latch data from an external device into the input register when a 74LS374 or 74LS373 latch is used. This line also sets the status flag so that the processor can tell if data has been entered.

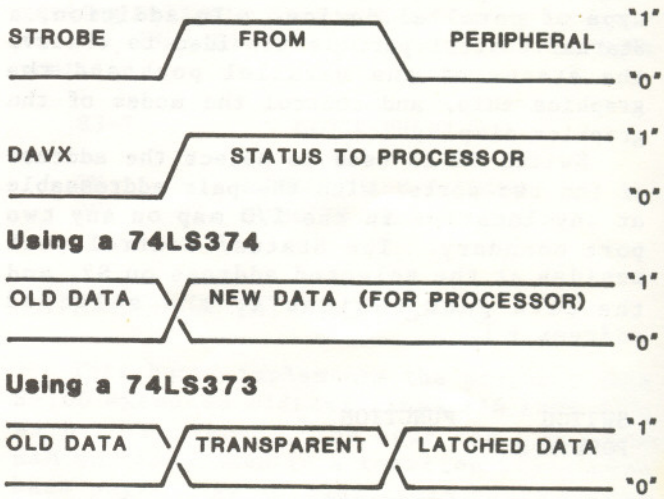
If a 74LS374 is used as the input register, a transition on the STROBE line latches the data and sets the status flag. The STROBE POLARITY SELECT SWITCH (S4) should be set as described below so that the peripheral's data is valid during the transition. With the select switch (S4) in the center position, a low to high transition on STROBE will latch the data. With the select switch set to the extreme left or right, a high to low transition on STROBE will latch the data.

If a 74LS373 is used as the input register, the strobe line can assume two different modes. The first mode is similar to the latched mode of the 74LS374 described above except that during the strobe pulse the data is transparent through the latch to the processor. At the end of the strobe pulse, the data will be latched and stable for the processor to access. With the STROBE POLARITY SELECT SWITCH (S4) in the center position, a positive going strobe pulse will latch the data at the end of the pulse. With the select switch in the extreme left or right position, a negative going strobe pulse will latch the data at the end of the pulse.

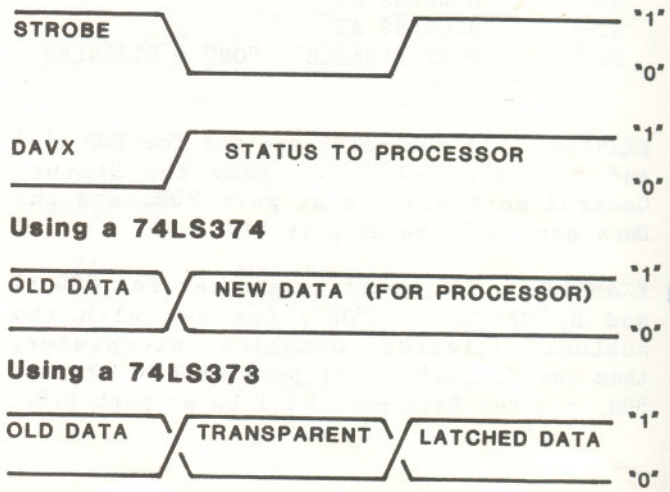
The second mode is the fully transparent mode where the data is never latched but is available for inputting at any time by the processor. This mode is useful whenever the data has no strobe bit associated with it. This mode is entered when the strobe line is left open with the strobe select switch in the center position. See the timing diagrams below for a visual representation of the input data and the strobe relationships

NOTE: In the diagrams below, the strobe is provided by the external device and the incoming data is shown as what is available to the processor in relation to the strobe pulse.

STROBE SELECT SWITCH "ON"



WITH STROBE SELECT SWITCH "OFF"



INPUT EXAMPLES

Some examples of typical applications might include connecting a ASCII keyboard or a set of sense switches to the input Channel of the SPECTRUM. A keyboard usually has a strobe line to indicate that it has current valid data on its data outputs. Therefore, using the 74LS374 latch would be best. The keyboard data lines would be connected accordingly to input data lines of the parallel Channel and the keyboard strobe line would be connected to the Channel STROBE input. The Strobe Select switch would be in the center position for a positive keyboard strobe, and to the extreme left or right for a negative keyboard strobe. If connecting some sense switches to the input lines, a 74LS373 would be the best choice because there are usually no strobe lines associated with switches. The switches should be connected to the input lines so that they ground the inputs (no pull-up resistors are needed since they are supplied on the board) and the STROBE LINE should be left floating with the Strobe Select switch in the center position. This allows the processor to input the data from the switches at any time. Another example of an input signal that usually does not have a strobe associated with it would be the Busy line and other status bits from a printer or other device.

OUTPUT ENABLE LINE

The OUTPUT ENABLE LINE on the Channel is used to Tri-State the output register and enable the Q and Q* output flags as described below. By Tri-Stating the output register, the user may bus the output data from several different sources onto the same 8 data lines. In this mode, the DNT status bit will stay high until the output register goes active, at which point the DNT status bit will go low. If the output register is active at all times, (most applications will be this way) the DNT status bit will stay low at all times.

When the Polarity Select Switch (S5) is in the center position, the OUTPUT ENABLE LINE must be low to enable the output register. With the Select Switch in the extreme left or right position, the OUTPUT ENABLE LINE must be high or left open to enable the output register.

ATTENTION LINE

The ATTENTION LINE is used to inform an external device that new data is now available for it. This line may be jumpered (J5) to provide any one of four different outputs. With the Common (C) jumpered to either Q or Q*, and the OUTPUT ENABLE LINE set so that the output of the register is Tri-Stated, then the ATTENTION LINE will go high (Q) or low (Q*) when data is strobed into the output register and the DNT status bit will go high. When the OUTPUT ENABLE LINE level is changed to enable the data, then the ATTENTION LINE will return to its original level and the DNT status bit will go low. In this mode, the OUTPUT ENABLE LINE is used to transfer the data out of the register and reset the attention flag. Since the level of the ATTENTION LINE may be sampled by the processor through the status port (DNT), a high speed handshaking data transfer can occur.

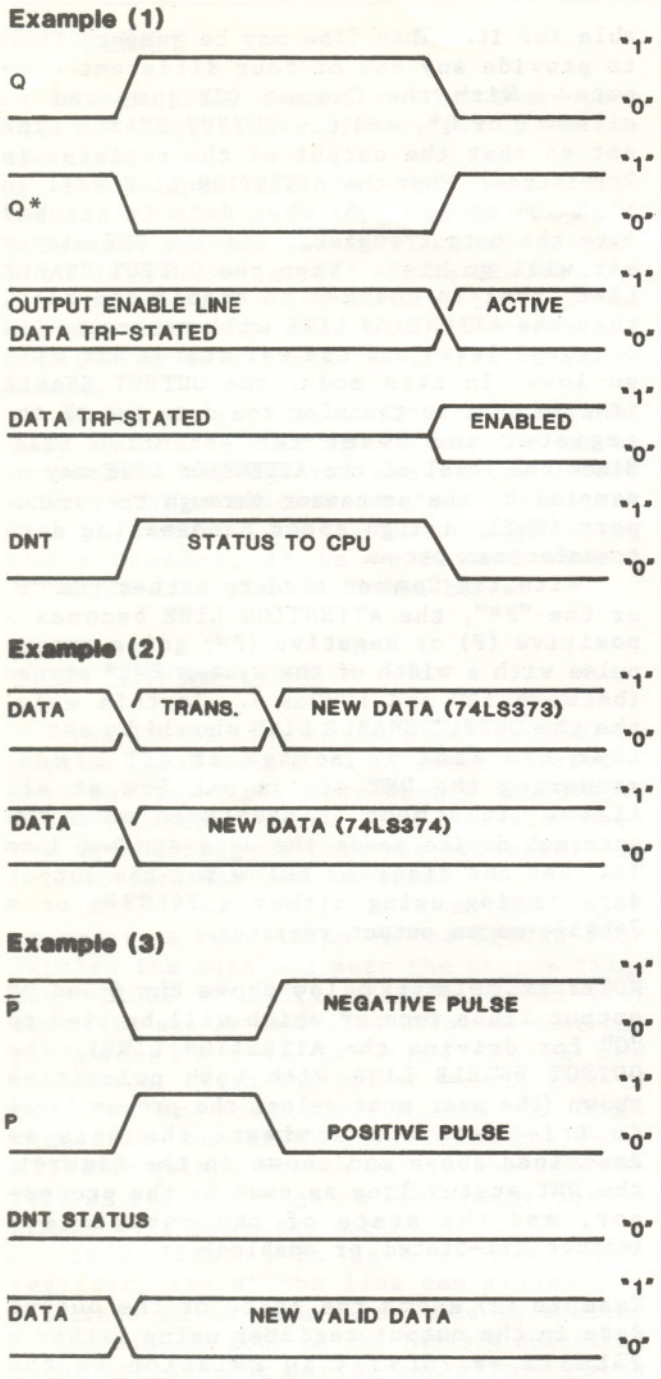
With the Common tied to either the "P" or the "P*", the ATTENTION LINE becomes a positive (P) or negative (P*) going strobe pulse with a width of the system PWR* strobe (between 150 and 1000ns). In this mode, the the OUTPUT ENABLE LINE should be set so that the data is active at all times, rendering the DNT status bit low at all times. This mode is best used when the external device needs the data strobed into it. See the diagrams below for the output data timing using either a 74LS373 or a 74LS374 as an output register.

NOTE: Example (1) below shows the Q and Q* output lines (one of which will be tied to "C" for driving the ATTENTION LINE), the OUTPUT ENABLE LINE with both polarities shown (the user must select the proper level to Tri-State and activate the data as described above and shown in the figure), the DNT status line as read by the processor, and the state of the output data (either Tri-Stated or enabled).

Example (2) shows the state of the output data in the output register using either a 74LS373 or 74LS374 in relation to the strobes in Examples (1) and (3). NOTE: The transparent time on the 74LS373 contains new valid data since the S-100 bus supplies valid data during this time.

Example (3) shows both the "P" and "P*" output pulses (one of which is tied to the "C" or Common line for generating a pulse on the ATTENTION LINE), the state of the new output data (either new or old data), and the DNT status line which is low to the processor at all times (assuming that the data is held active at all times with the OUTPUT ENABLE LINE).

OUTPUT DATA TIMING



OUTPUT EXAMPLE

Some examples of typical applications might include connecting a parallel printer or some LED's to the output lines. A parallel printer might require that 7, or 8 data lines be connected in addition to a strobe line. In many cases, the strobe (P or P*) connected to the ATTENTION LINE will be sufficiently long for the printer and can be connected directly with the proper polarity for correct printer operation. Some printers might require a longer strobe than the system PWR* pulse width, therefore a longer strobe can be made by switching a data bit on and off via software to act as a strobe. If only 7 data lines are required for the printer, then the eighth data line may be used and the software tailored to provide a strobe pulse of almost any length.

NOTE: Since the 74LS373 and 74LS374 octal latches are pin compatible, you may move either one into positions U18 and U19 on your board for your particular application.

I/O CONNECTOR PINOUTS

In addition to the 16 data lines and 3 control lines provided at the port connector, a small amount of current is available at the +5, +12, and -12 volt pins for powering external devices such as a keyboard or A to D converter. The total current is shown below, and care must be taken not to exceed these rating and overheat the regulators.

+ 5 volts @ 150 ma.
+12 volts @ 40 ma.
-12 volts @ 40 ma.

DB-25 PIN NUMBERS & SIGNAL NAMES

1- -12 VOLTS	13- +12 VOLTS
2- DATA IN 0	14- GROUND
3- DATA IN 22	15- DATA IN 1
4- DATA IN 4	16- DATA IN 3
5- DATA IN 6	17- DATA IN 5
6- STROBE	18- DATA IN 7
7- +5 VOLTS	19- GROUND
8- ATTENTION	20- GROUND
9- DATA OUT 0	21- ENABLE
10- DATA OUT 2	22- DATA OUT 1
11- DATA OUT 4	23- DATA OUT 3
12- DATA OUT 6	24- DATA OUT 5
	25- DATA OUT 7

COLOR GRAPHICS MODES

The SPECTRUM board will initially power-up as an 8K RAM board, and consequently must be told to enter the color graphics mode. To accomplish this, a logic "1" must be sent to data bit 5 of the CONTROL port. To exit from graphics mode back to RAM mode, a logic "0" should be sent to data bit 5 of the CONTROL port or the reset switch on your computer may be pressed which clears the CONTROL port to the power-up state.

Once in graphics mode, the CONTROL port may be altered to enter into any of the nine available modes of operation described below.

DATA BIT						MODE
D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	RAM MODE
1	X	0	X	X	X	ALPHA/SEMIGRAPHICS
1	0	X	X	X	X	COLOR SET A
1	1	X	X	X	X	COLOR SET B
1	X	1	0	0	0	64 X 64 COLOR GRAPHICS
1	X	1	0	0	1	128 X 64 GRAPHICS
1	X	1	0	1	0	128 X 64 COLOR GRAPHICS
1	X	1	0	1	1	128 X 96 GRAPHICS
1	X	1	1	0	0	128 X 96 COLOR GRAPHICS
1	X	1	1	0	1	128 X 192 GRAPHICS
1	X	1	1	1	0	128 X 192 COLOR GRAPHICS
1	X	1	1	1	1	256 X 192 GRAPHICS

"X" = don't care

ALPHA/SEMIGRAPHICS MODE

The 6847 contains an internal character generator capable of displaying 64 ASCII characters in a 32 character per line/ 16 line format. These characters may be displayed in normal or inverted video on a character by character basis. Also, the 6847 is capable of entering a course graphics mode called SEMIGRAPHICS 4. In this mode, each character position becomes a rectangle of eight by twelve dots that is divided into four parts. The luminance of each of the four parts (L0 - L3), and the color of the rectangle (C0 - C2) is controlled as shown in a following section.

ALPHANUMERIC DATA FORMAT

The alphanumeric data shown below should be configured as shown below in the sample data word. To display a standard video character, data bit 6 should be a "0". For an inverted character, data bit 6 should be a "1". To display alphanumeric characters, data bit 7 should be a "0", and to enter SEMIGRAPHICS 4 mode, data bit 7 should be a "1".

DATA BIT	ALPHA FORMAT	SEMIGRAPHICS FORMAT
D0	DATA 0	L0
D1	DATA 1	L1
D2	DATA 2	L2
D3	DATA 3	L3
D4	DATA 4	C0
D5	DATA 5	C1
D6	INVERT	C2
D7	0	1

SEMIGRAPHICS FORMAT

In SEMIGRAPHICS format, data bit 7 (D7) must be a "1" as shown below. The data bits will control the luminance (Lx) of the sub-square, and the color (Cx) of all four four squares as shown below in the four square pixel map.

PIXEL MAP

L3	L2
L1	L2

DATA BIT FUNCTION MAP

D7	D6	D5	D4	D3	D2	D1	D0
1	C2	C1	C0	L3	L2	L1	L0

"L" = "0" = COLOR OFF
"L" = "1" = COLOR ON

COLOR BITS			INTENSITY	COLOR
C2	C1	C0	Lx	SELECTED
X	X	X	0	BLACK
0	0	0	1	GREEN
0	0	1	1	YELLOW
0	1	0	1	BLUE
0	1	1	1	RED
1	0	0	1	BUFF(GRAY)
1	0	1	1	CYAN
1	1	0	1	MAGENTA
1	1	1	1	ORANGE

ALPHANUMERICS CHARACTER SET

HEX DATA	ASCII CHAR	HEX DATA	ASCII CHAR	HEX DATA	ASCII CHAR	HEX DATA	ASCII CHAR
00H	@	10H	P	20H	(SP)	30H	0
01H	A	11H	Q	21H	!	31H	1
02H	B	12H	R	22H	"	32H	2
03H	C	13H	S	23H	#	33H	3
04H	D	14H	T	24H	$	34H	4
05H	E	15H	U	25H	%	35H	5
06H	F	16H	V	26H	&	36H	6
07H	G	17H	W	27H	'	37H	7
08H	H	18H	X	28H	(	38H	8
09H	I	19H	Y	29H	)	39H	9
0AH	J	1AH	Z	2AH	*	3AH	:
0BH	K	1BH	[	2BH	+	3BH	;
0CH	L	1CH	\	2CH	,	3CH	<
0DH	M	1DH	]	2DH	-	3DH	=
0EH	N	1EH	^	2EH	.	3EH	>
0FH	O	1FH	<-	2FH	/	3FH	?

NOTE: To display ASCII data in ALPHA mode on your SPECTRUM board, a 40H bias must be subtracted from ASCII codes 40H thru 7FH to form the compacted 6 bit code for the 6847's internal character generator.

COLOR GRAPHICS BIT MAPPING

Modes described above as COLOR GRAPHICS modes will have their data bits mapped out on the screen as described below. The pixels are mapped across the screen, starting with byte 0 of the graphics RAM, from the upper left corner of the T.V. picture - across then down - to the lower right corner of the picture.

```
PIXEL NUMBER          COLOR MAP
------------      ------------------------
|E3|E2|E1|E0|     | E3  | E2  | E1  | E0  |
------------      ------------------------
    COLOR BIT -|C1|C0|C1|C0|C1|C0|C1|C0|
               ------------------------
     DATA BIT -|D7|D6|D5|D4|D3|D2|D1|D0|
               ------------------------
```

CSS = "0"			CSS = "1"		
C1	C0	COLOR	C1	C0	COLOR
0	0	GREEN	0	0	BUFF (GRAY)
0	1	YELLOW	0	1	CYAN
1	0	BLUE	1	0	MAGENTA
1	1	RED	1	1	ORANGE
BORDER = GREEN			BORDER = BUFF (GRAY)		

GRAPHICS BIT MAPPING

Modes described above as GRAPHICS modes will have their data bits mapped out on the screen as described below. The pixels are mapped across the screen, starting with byte 0 of the graphics RAM, from the upper left corner of the T.V. picture - across then down - to the lower right corner of the picture. In this mode, each data bit maps directly into a pixel as shown.

```
  PIXEL/INTENSITY MAP
 ----------------------
|L7|L6|L5|L4|L3|L2|L1|L0|    INTENSITY BIT
|--|--|--|--|--|--|--|--|
|D7|D6|D5|D4|D3|D2|D1|D0|    DATA BIT
 ----------------------
```

CSS = "0"		CSS = "1"	
LX	COLOR	LX	COLOR
0	BLACK	0	BLACK
1	GREEN	1	BUFF (GRAY)
BORDER = GREEN		BORDER = BUFF (GRAY)	

COLOR GRAPHICS MODE DESCRIPTION SUMMARY

HORIZ	VERT	BITS/ PIXEL	MAX/RAM	GM2	GM1	GM0
64	64	2	1K BYTE	0	0	0
128	64	2	2K BYTES	0	1	0
128	96	2	3K BYTES	1	0	0
128	192	2	6K BYTES	1	1	0

GRAPHICS MODE DESCRIPTION SUMMARY

HORIZ	VERT	BITS/ PIXEL	MAX/RAM	GM2	GM1	GM0
128	64	1	1K BYTE	0	0	1
128	96	1	1.5K BYTES	0	1	1
128	192	1	3K BYTES	1	0	1
256	192	1	6K BYTES	1	1	1

USING THE 6847 STATUS BITS

The 6847 provides two status lines to inform the user that it is currently scanning a non-active portion of the display. This provides a convenient way for the user to update the display without causing any noticeable flicker or tearing of the picture. To accomplish this, the user must test the HS* and the FS* signals from the status port. Care must be taken to test these bits properly, as they are active low signals.

NAME	MEANING & DESCRIPTION	DATA BIT	PULSE WIDTH
HS*	HORIZ. SYNCPERIOD	D6	4.9us
FS*	VERT. SYNC PERIOD	D7	1.6ms

INITIAL ADJUSTMENTS

As shipped, the SPECTRUM board should require no initial adjustments. However, as components age and change values, the initial adjustment of variable capacitor C15 may need to be altered in order to provide the proper colors described in a previous section. At this point, the user should fill the screen with some large areas of solid color. For example, in SEMIGRAPHICS mode, fill two lines with each color so that all 8 colors are visible, and adjust C15 so that the proper colors appear in the proper locations.

If the optional 10K ohm resistor R5 has been installed, it may be adjusted with an oscilloscope until the clock signal (pin 8, U25) is a square wave. If an oscilloscope is unavailable, adjust it until ALPHANUMERIC characters are as clear as possible. At this point, no other adjustments need to be made on the board.

PICTURE ADJUSTMENTS

For the best possible picture, minor adjustments will probably need to be made to the color monitor or television.

Monitors will most likely require adjustment of the Video Level control and the Video Offset control (if provided) for the sharpest picture. The Tint control should be adjusted if C15 did not provide enough range, and the Color control should be adjusted for the most attractive color saturation and picture quality possible. Brightness and Contrast should be adjusted to provide the clearest characters and most pleasing display.

Color televisions with R.F. modulators should follow the same instuctions as above, except that the Video Level adjustment will probably be on the R.F. modulator unit.

VIDEO OUTPUT CONNECTORS

1. J1 - RCA JACK

RCA connector J1 provides 75 ohm video output for connection to a video monitor or television that requires a composite video signal. Care should be taken to insure a clean signal by using coaxial cable for the interconnection. The signal provided by this output is approximately 1.5 volts peak to peak, with sync tips at 0 volts, black at 0.7 volts and white at 1.5 volts. Keep in mind that these values are only approximate, and that component variations will cause these levels to shift a small amount.

2. J4 - FOUR PIN MALE CONNECTOR

The four pin connector at J4 is provided for interfacing to F.C.C approved R.F. type modulators. The pin connections on the SPECTRUM board are listed below, and will mate directly with some commercially available modulators.

PIN NUMBER	SIGNAL
1	GROUND
2	75 ohm VIDEO
3	NO CONNECTION
4	+ 12 VOLTS

NOTE: Always insure that if using an R.F. modulator, that you use an F.C.C. approved type with an isolation switch. If not using an isolation switch, make sure that you completely remove your antenna lead in from the terminals on your television.

FOR BEST RESULTS.....

If not using a computer grade color monitor for displaying the output of your SPECTRUM board, a good quality television is a must. The old clunker that nobody wanted and the $149 wonder at the discount store probably won't give you the quality picture that you want to see. So, if your going to buy a television, new or used, get a good quality one that is 100% solid state, has good high voltage regulation, has a transformer (for safety's sake!), and has D.C. restored video. Look for one that has a sharpness control and a control called Black Level (this is a good indication that the set has D.C. video restoration). Zenith, RCA, and SONY make excellent small color televisions that are a great addition to any home when not used for color graphics.

CIRCUIT DESCRIPTION

The heart of the SPECTRUM board consists of a MOS LSI color video display generator. This display generator performs the scanning of the refresh display RAM and processes the fetched data into NTSC compatible color video signals for display on standard televisions and monitors. For an understanding of the operation of SPECTRUM, it can be roughly broken down into five separate subsections: the INTERNAL DATA BUS, the MEMORY DECODE LOGIC, the INTERNAL ADDRESS BUS, the PARALLEL I/O PORTS AND LOGIC, and the GRAPHICS GENERATOR AND VIDEO CIRCUITRY.

INTERNAL DATA BUS

The INTERNAL INPUT DATA BUS consists of octal input buffer U21, which provides buffered data to the RAM, the PARALLEL I/O PORT and the GRAPHICS CONTROL PORT. This bus is active at all times, and data is latched from it only when the RAM or I/O ports are selected.

The INTERNAL OUTPUT DATA BUS is directly connected to the S-100 DI bus, and is driven by three separate output buffers. The RAM output is driven through octal buffer U20, the parallel data is driven through octal latch U18, and the board status through hex buffer U32. All three of these buffers remains in the TRI-STATE condition until selected, and all are capable of 24ma. drive current.

MEMORY DECODE LOGIC

The MEMORY DECODE LOGIC consists of circuitry that detects a board select, and circuitry that decodes valid RAM strobe signals. The board select logic consists primarily of U34 and U24, which decode A13-A15 for the RAM address, sINP and sOUT for memory reference, ADDRESS EXTEND for 24 bit addressing and PHANT* for PHANTOM decode. This signal is further gated with BSVAL and R*/G to decode a Valid Board Select (VBS) signal when in GRAPHICS mode. In RAM mode, BSVAL is ignored when generating VBS.

Valid RAM strobe signals are generated by gating VBS with pDBIN and sMEMR for RAM Data Output Enable (RAM DOEN*) and pWR* and MWRT for WRITE ENABLE (WE*). These are used to enable the RAM data output buffer and write data into the RAM respectively.

In graphics mode, a wait state is left pending in U26, and is gated onto the bus (U35 and U29) when enabled and SEL is active. The wait state is clocked out on the next edge of the bus clock after the start of STROBE*.

INTERNAL ADDRESS BUS

The INTERNAL ADDRESS BUS is a dual bus that can be controlled by the 6847 GRAPHICS GENERATOR or by the S-100 bus. In normal operation, the 6847 has control of the address lines since it is constantly scanning the memory for display information, and the S-100 address drivers, U36 and U37, are TRI-STATED. When the RAM is accessed by the host computer, the 6847 address bus is TRI-STATED and the S-100 address drivers are given control to perform a memory read or write. As soon as this action is completed, the 6847 regains control of the address bus. (NOTE: since the 6847 depends on a constant stream of picture data from the RAM, accessing the display RAM during active display time will cause disruption of the display as incorrect data is forced onto the data bus. It is best to access the RAM during inactive display time as no picture disruption will occur.)

PARALLEL I/O PORTS & DECODE LOGIC

The I/O ports are enabled when octal comparator U33 decodes the proper address on the S-100 bus and decoder IC31 determines that an I/O read or write is occuring. The four decoded signals select whether a data or status read or a data or control write is to occur. In the read case, this signal is used to gate the data onto the S-100 bus, and in the write case, this signal is used to latch the data into the appropriate register.

The external data input register, U18, is an octal latch fed by the X-OR gate (U22) acting as a programmable inverter. As data is latched into the register by a transition on the STROBE LINE, the DAV flag bit is set (U23) to inform the processor that new data has been entered. The flag is cleared and data gated onto the bus when an I/O data read occurs.

The external data output register, U19, is an octal latch that accepts data when an I/O data write occurs. At the same time, the ATTENTION flag is set to inform an external device that that new data is available. The OUTPUT ENABLE line is fed through an X-OR (U22) acting as a programmable inverter to enable the output data and reset the ATTENTION flag.

The graphics control data is latched into hex latch (U30) by a transition on the I/O control write line (CNRL WR*) and the status is gated onto the data bus through U32 with the I/O status read signal (STAT RD*).

GRAPHICS GENERATOR & VIDEO CIRCUITRY

The 6847 graphics generator (U29), scans the address bus and fetches the data made available on the data bus. The outputs provided include several status/ timing signals in addition to the composite video and color vector voltages used by chroma encoder U1 (1372). The chroma encoder provides the main timing clock for the graphics generator and encodes the composite video and color vectors into a NTSC color encoded signal that is buffered to provide a low impedance video output. Crystal X1 forms the basis for a precise 3.579545 MHz oscillator and Q1 and Q2 buffer the video output of the 1372 to provide a 75 ohm output impedance for connection to a monitor or an F.C.C approved R.F. modulator.

MEMORY TESTING

If the memory board seems to be working properly, the Memory Testing Routine (figure 1) can be used to give the board a more thorough workout. It is rather slow; but will do the job well. It can be entered via editor/assembler or front panel switches.

The routine is set up to test 8K from 4000 hex up to 6000 hex. This may be changed by entering a different starting address at "STRT" (3001 - 3002) and/or a different end address at "END" (3004 - high order byte only).

If the memory passes the test it starts over again. You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart.

If the memory fails the test, critical information is stored and the routine enters a software "HALT", that is a "jump to here" at "SHLT". Front panel lights, if any, will show this state. The user may then use the front panel or dump routines to display the following stored failure info:

3069* "FDE" = D, E pair . . . D is the fill character and E is the test character
306B* "FHL" = H, L pair . . . the failure address
306D* "FOUT" = the data expected at this address
306E* "FIN" = the data read from, the address
* address from *Memory Testing Routine Listing.*

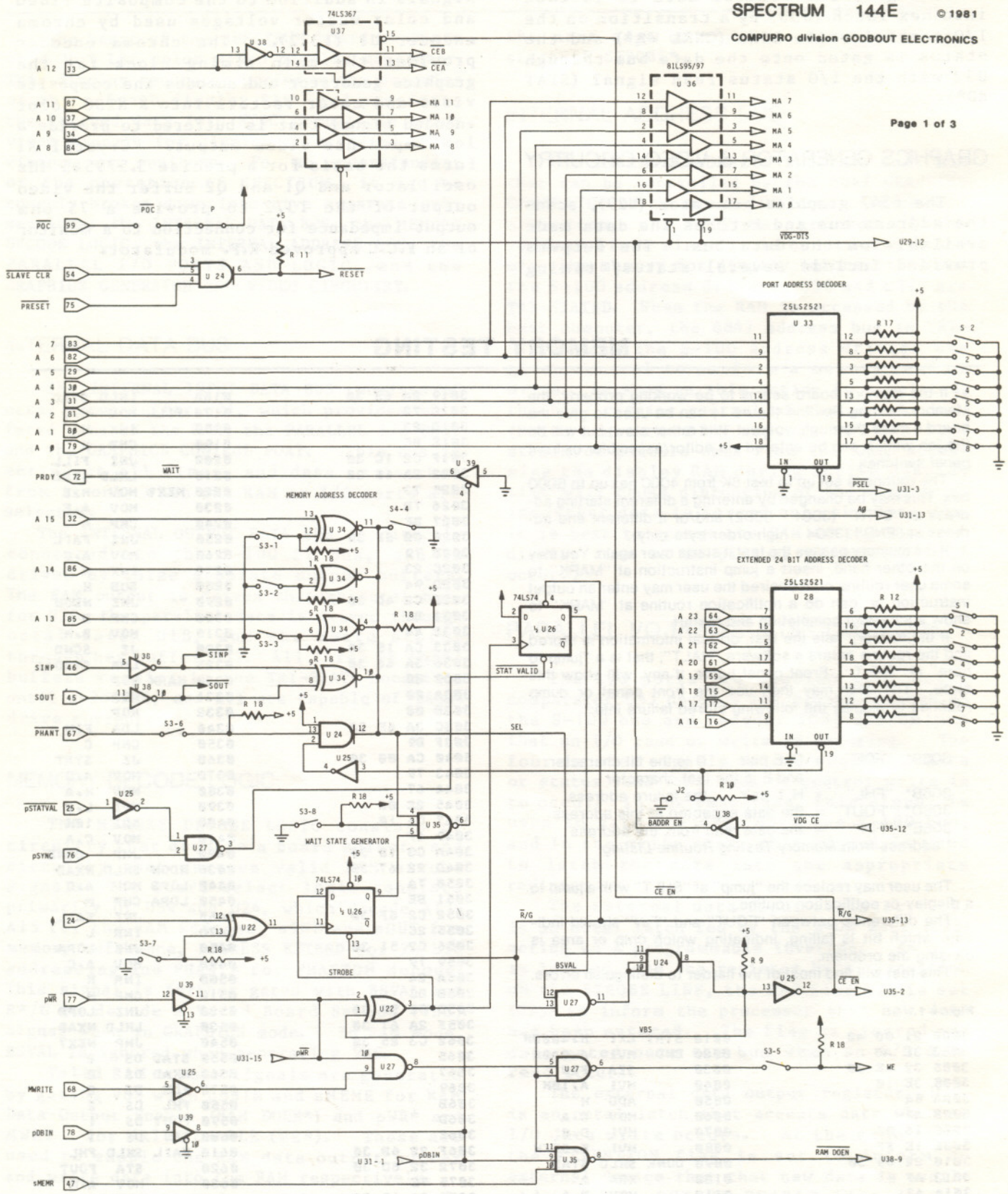
The user may replace the "jump" at "SHLT" with a jump to a display or notification routine.

The difference between "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem.

This test will find most of the harder to distinguish errors.

Figure 1.

```
3000 21 00 40          0010 STRT LXI  H,4000H
3003 3E A0             0020 END  MVI  A,0A0H
3005 32 6E 30          0030      STA  FIN
3008 3E 10             0040      MVI  A,10H
300A 84                0050      ADD  H
300B 4F                0060      MOV  C,A
300C 16 00             0070      MVI  D,0
300E 1E FF             0080      MVI  E,0FFH
3010 22 65 30          0090 DONE SHLD STAD
3013 AF                0100      XRA  A
3014 47                0110      MOV  B,A
3015 7B                0120 SCND MOV  A,E
3016 5A                0130      MOV  E,D
3017 57                0140      MOV  D,A
3018 79                0150      MOV  A,C
3019 2A 65 30          0160      LHLD STAD
301C 72                0170 FILL MOV  M,D
301D 23                0180      INX  H
301E BC                0190      CMP  H
301F C2 1C 30          0200      JNZ  FILL
3022 2A 65 30          0210      LHLD STAD
3025 73                0220 NEXT MOV  M,E
3026 7B                0230      MOV  A,E
3027 BE                0240      CMP  M
3028 C2 6F 30          0250      JNZ  FAIL
302B 79                0260      MOV  A,C
302C 23                0270      INX  H
302D 94                0280      SUB  H
302E C2 4D 30          0290      JNZ  NDON
3031 B8                0300      CMP  B
3032 44                0310      MOV  B,H
3033 CA 15 30          0320      JZ   SCND
3036 3A 66 30          0325      LDA  STAD+1
3039 00                0330 MARK NOP
303A 00                0331      NOP
303B 00                0332      NOP
303C 3A 6E 30          0340      LDA  FIN
303F B9                0350      CMP  C
3040 CA 00 30          0360      JZ   STRT
3043 79                0370      MOV  A,C
3044 67                0380      MOV  H,A
3045 2E 00             0390      MVI  L,0
3047 C6 10             0400      ADI  10H
3049 4F                0410      MOV  C,A
304A C3 10 30          0420      JMP  DONE
304D 22 67 30          0430 NDON SHLD NXAD
3050 7A                0440 LOPB MOV  A,D
3051 BE                0450 LOPA CMP  M
3052 C2 6F 30          0460      JNZ  FAIL
3055 2C                0470      INR  L
3056 C2 51 30          0480      JNZ  LOPA
3059 79                0490      MOV  A,C
305A 24                0500      INR  H
305B BC                0510      CMP  H
305C C2 50 30          0520      JNZ  LOPB
305F 2A 67 30          0530      LHLD NXAD
3062 C3 25 30          0540      JMP  NEXT
3065                   0550 STAD DS   2
3067                   0560 NXAD DS   2
3069                   0570 FDE  DS   2
306B                   0580 FHL  DS   2
306D                   0590 FOUT DS   1
306E                   0600 FIN  DS   1
306F 22 6B 30          0610 FAIL SHLD FHL
3072 32 6D 30          0620      STA  FOUT
3075 7E                0630      MOV  A,M
3076 32 6E 30          0640      STA  FIN
3079 EB                0650      XCHG
307A 22 69 30          0660      SHLD FDE
307D C3 7D 30          0670 SHLT JMP  SHLT
3080                   0680 *
```


74LS367
U37
U38
CEB
CEA
A 12
A 11
A 10
A 9
A 8
MA 11
MA 10
MA 9
MA 8
81LS95/97
U36
MA 7
MA 6
MA 5
MA 4
MA 3
MA 2
MA 1
MA 0
VDG-DTS
U29-12
POC
SLAVE CLR
PRESET
U24
R 11
RESET
PORT ADDRESS DECODER
25LS2521
U33
R 17
S 2
IN
OUT
PSEL
U31-3
A0
U31-13
A 7
A 6
A 5
A 4
A 3
A 2
A 1
A 0
PRDY
WAIT
U39
MEMORY ADDRESS DECODER
S4-4
A 15
A 14
A 13
S3-1
S3-2
S3-3
U34
R 18
SINP
SOUT
PHANT
S3-6
74LS74
½ U26
STAT VALID
SEL
EXTENDED 24 BIT ADDRESS DECODER
25LS2521
U28
R 12
S 1
A 23
A 22
A 21
A 20
A 19
A 18
A 17
A 16
J2
R 10
BADDR EN
VDG CE
U35-12
pSTATVAL
pSYNC
U27
U25
S3-8
U35
WAIT STATE GENERATOR
74LS74
½ U26
U22
S3-7
STROBE
CE EN
R/G
U35-13
BSVAL
U24
R 9
U35-2
pWR
U31-15
VBS
S3-5
WE
MWRITE
pDBIN
U31-1
RAM DOEN
U38-9
sMEMR

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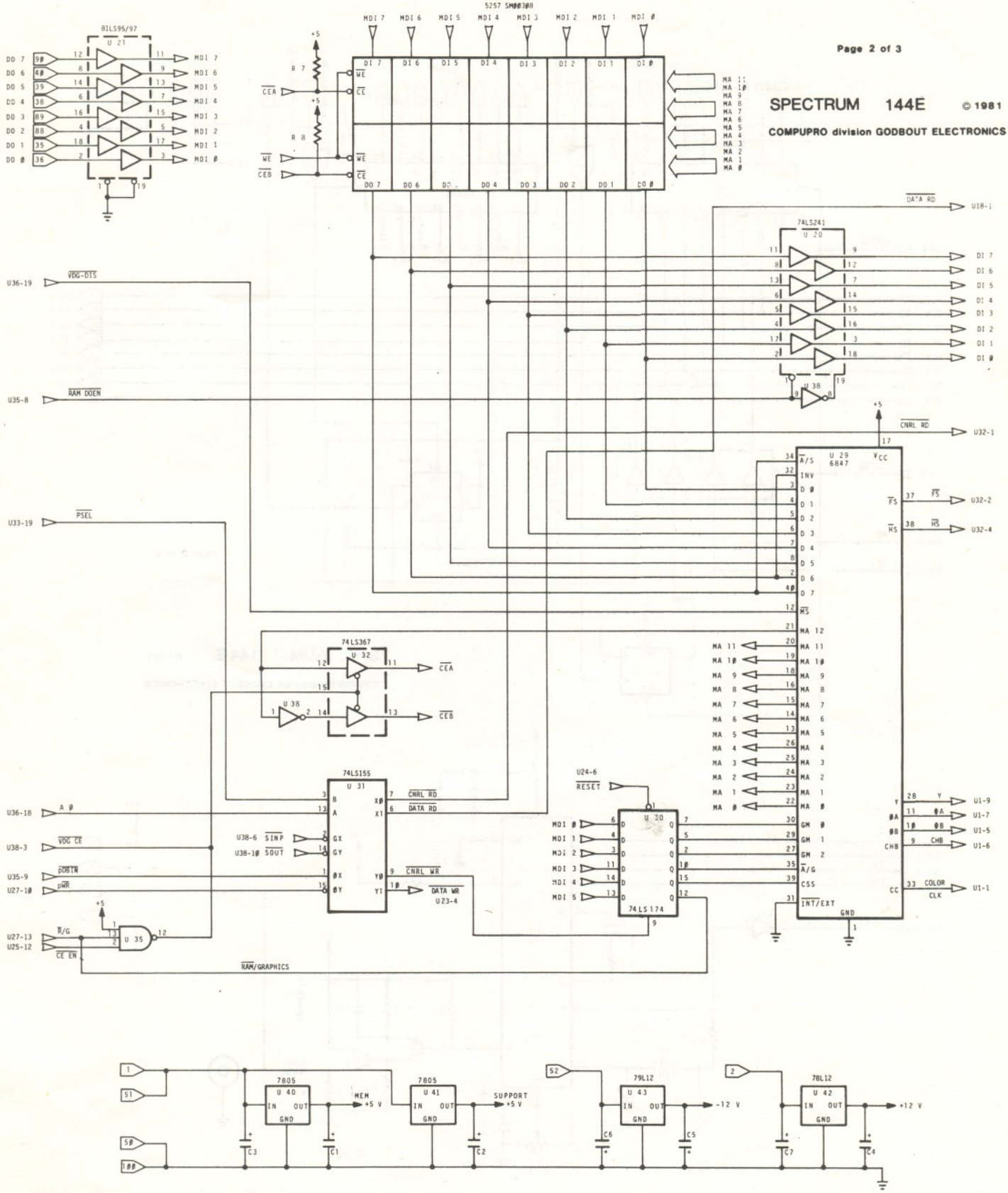
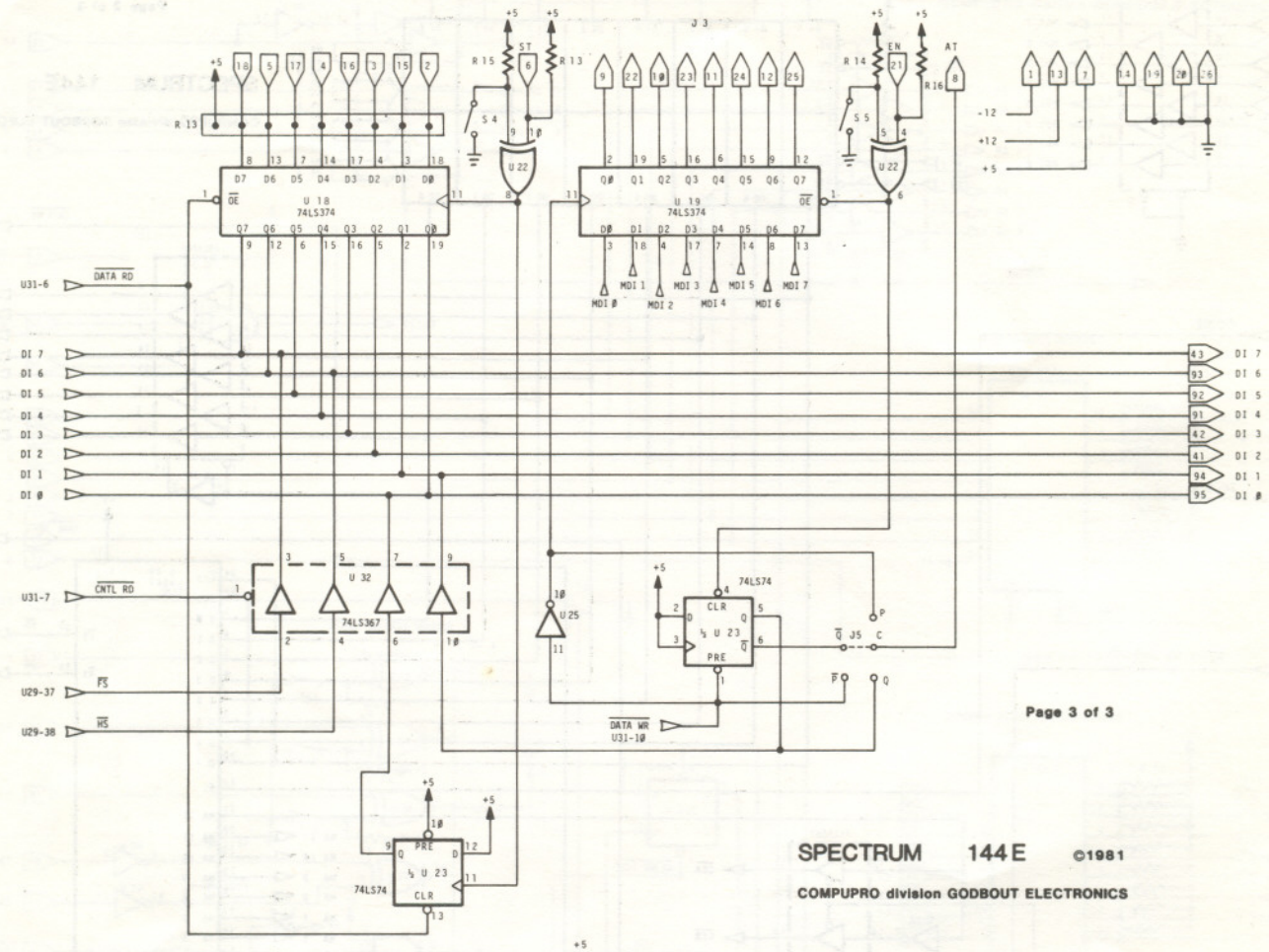
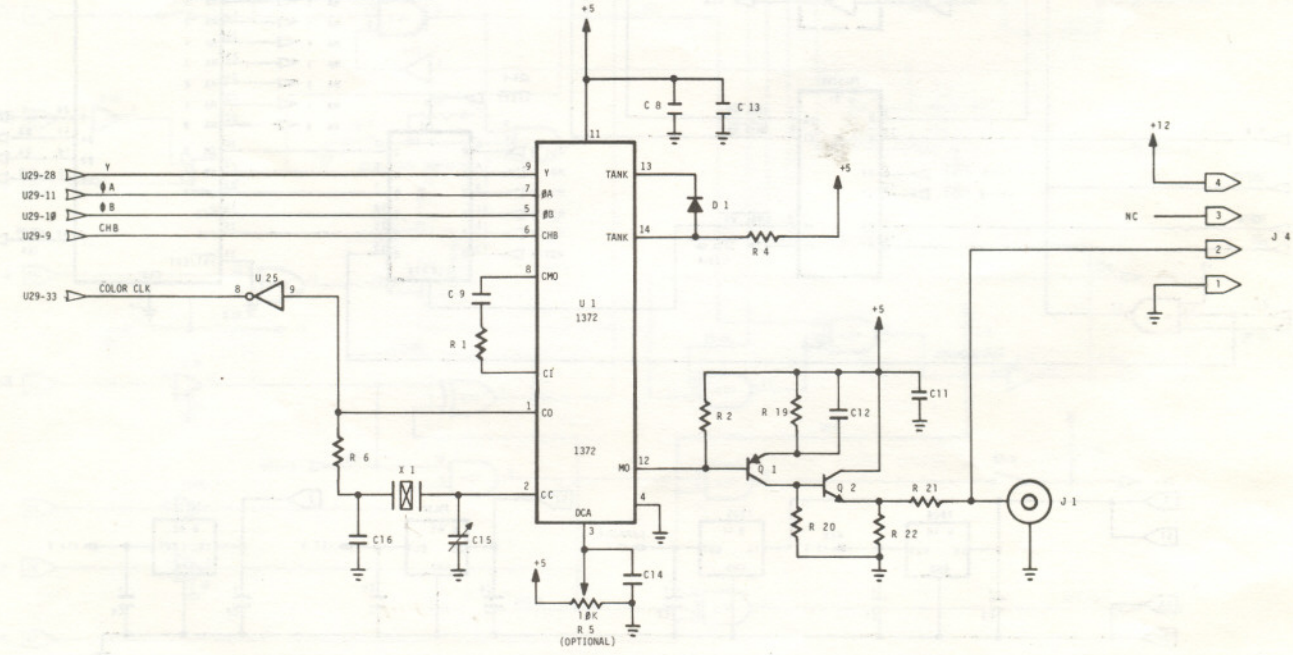



J 3
R 13
R 15
R 14
R 16
S 4
S 5
U 22
U 18
74LS374
U 19
74LS374
MDI Ø
MDI 1
MDI 2
MDI 3
MDI 4
MDI 5
MDI 6
MDI 7
U31-6 DATA RD
DI 7
DI 6
DI 5
DI 4
DI 3
DI 2
DI 1
DI Ø
U31-7 CNTL RD
U 32
74LS367
U25
74LS74
U29-37 FS
U29-38 HS
DATA WR
U31-1Ø
Page 3 of 3


SPECTRUM 144E ©1981
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U29-28 Y
U29-11 ØA
U29-1Ø ØB
U29-9 CHB
U29-33 COLOR CLK
U 1
1372
C 8
C 13
D 1
R 4
C 9
R 1
R 6
X 1
C16
C15
C14
1ØK
R 5
(OPTIONAL)
R 2
R 19
C12
C11
Q 1
Q 2
R 21
R 20
R 22
J 1
J 4
NC

NOTES

Parts List

[] (1) Circuit board

INTEGRATED CIRCUITS (NOTE: the following parts may have letter suffixes and prefixes along with the key numbers given below).

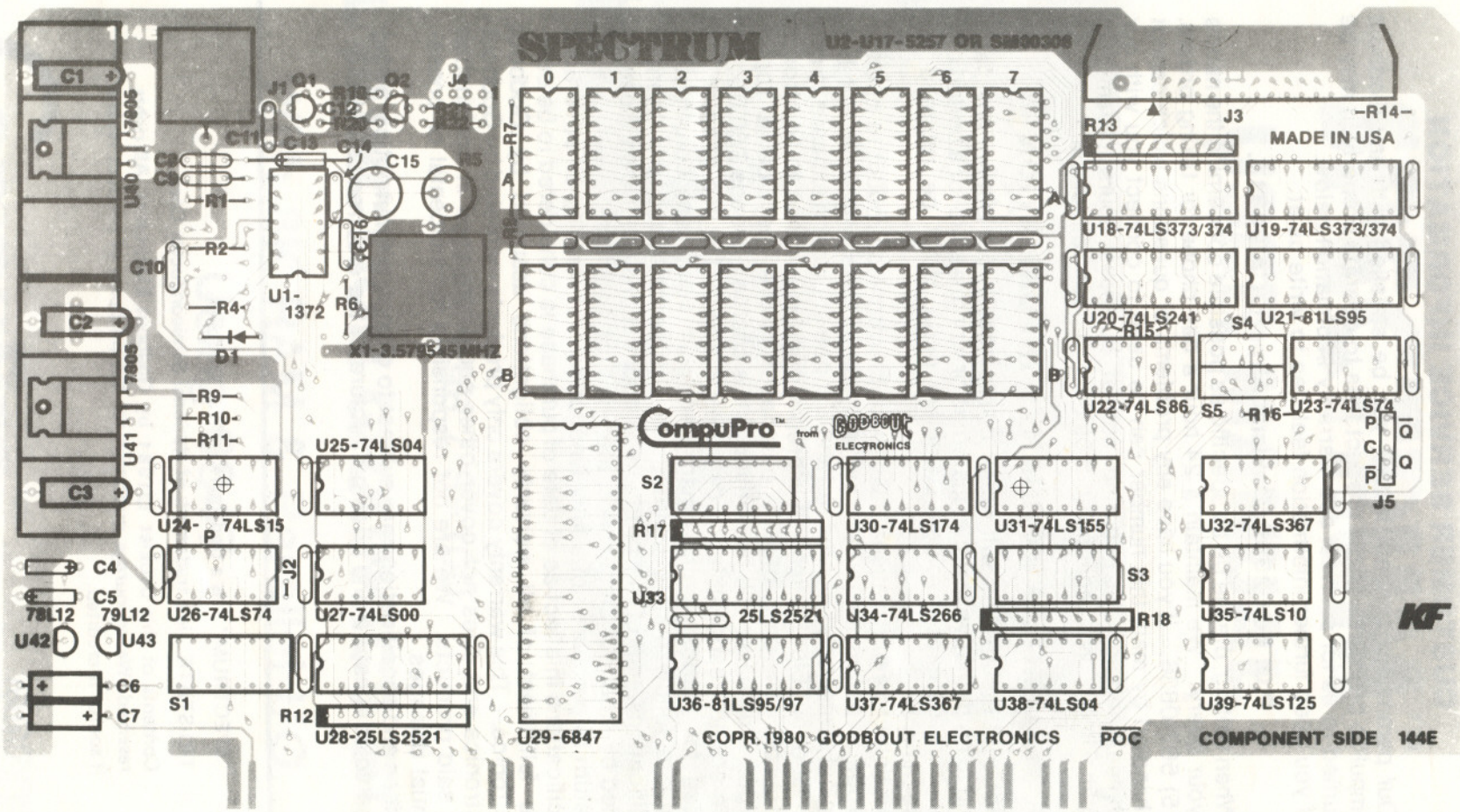
[]	(1)	74LS00	quad 2 input NAND	(U27)
[]	(2)	74LS04	hex inverter	(U25,U38)
[]	(1)	74LS10	triple 3 input NAND	(U35)
[]	(1)	74LS15	triple 3 in. OC NAND	(U24)
[]	(2)	74LS74	dual D flip flop	(U23,U26)
[]	(1)	74LS86	quad X-OR	(U22)
[]	(1)	74LS125	quad TS buffer	(U39)
[]	(1)	74LS155	decoder	(U31)
[]	(1)	74LS174	hex register	(U30)
[]	(1)	74LS241	octal bus driver	(U20)
[]	(2)	74LS367	hex TS buffer	(U32,U37)
[]	(1)	74LS373	octal latch	(U18)
[]	(1)	74LS374	octal latch	(U19)
[]	(2)	81LS95	octal bus driver	(U21,U36)
[]	(2)	25LS2521	octal comparator	(U28,U33)
[]	(16)	2147	4K x 1 static RAM	(U2-U17)
[]	(1)	6847	color graphics gen.	(U29)
[]	(1)	1372	color video encoder	(U1)
[]	(2)	7805	5 volt regulator	(U40,U41)
[]	(1)	78L12	12 volt regulator	(U42)
[]	(1)	79L12	-12 volt regulator	(U43)

OTHER ELECTRICAL COMPONENTS

[]	(1)	2N3906 transistor	(Q1)
[]	(1)	2N3904 transistor	(Q2)
[]	(1)	1N4148 or similar diode	(D1)
[]	(1)	crystal, 3975.545 Khz	(X1)
[]	(1)	trimmer capacitor	(C15)
[]	(3)	39uf, 10v tant. cap.	(C1-3)
[]	(3)	3.3uf, 15v tant. cap.	(C4,5,13)
[]	(2)	1.8uf, 35v tant. cap.	(C6,7)
[]	(1)	.1uf disc cap.	(C9)
[]	(4)	.01uf disc cap.	(C8,C10,C11,C14)
[]	(1)	100pf disc cap.	(C12)
[]	(1)	47pf disc cap.	(C16)
[]	(29)	disc caps.	
[]	(1)	56 ohm res.	(R21)
[]	(1)	360 ohm res.	(R4)
[]	(2)	750 ohm res.	(R1,R19)
[]	(3)	1K ohm res.	(R7,8,22)
[]	(1)	1.8K ohm res.	(R2)
[]	(6)	2.7K ohm res.	(R9-11,R14-16)
[]	(1)	3.3K ohm res.	(R20)
[]	(1)	5.6K ohm res.	(R6)
[]	(4)	SIP res. packs	(R12,13,17,18)

MECHANICAL COMPONENTS

[]	(39)	low profile sockets	
[]	(3)	dipswitches	(S1,S2,S3)
[]	(2)	slide switches	(S4,S5)
[]	(2)	heat sinks	
[]	(2)	sets 6-32 hardware	
[]	(1)	26 pin I/O connector	(J3)
[]	(1)	RCA connector	(J1)
[]	(1)	4 pin male connector	(J4)
[]	(1)	instuction booklet	



Component Layout

288 6121

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If you need further information feel free to write us at:

P.O. Box 2355, Oakland Airport, CA 94614.

When writing, please be as specific as possible concerning the nature of your query. We maintain a 24 hour a day phone for taking orders, (415) 562-0636. If you have any problems or questions which cannot be handled by mail, this number can be used to connect you with our technical people ONLY during normal business hours (10am-5pm Pacific Time). We cannot return calls or accept collect calls.

LIMITED WARRANTY INFORMATION

Godbout Electronics will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of 1 year from date of invoice. Defective parts *MUST* be returned for replacement.

If a defective part causes a Godbout Electronics product to operate improperly during the 1 year warranty period, we will service it free (original owner only) if delivered and shipped at owner's expense to and from Godbout Electronics. If improper operation is due to an error or errors on the part of the purchaser, there may be a repair charge. Purchaser will be notified if this charge exceeds $50.00.

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